

Fig. 1

200

T06290" T4096860

Database

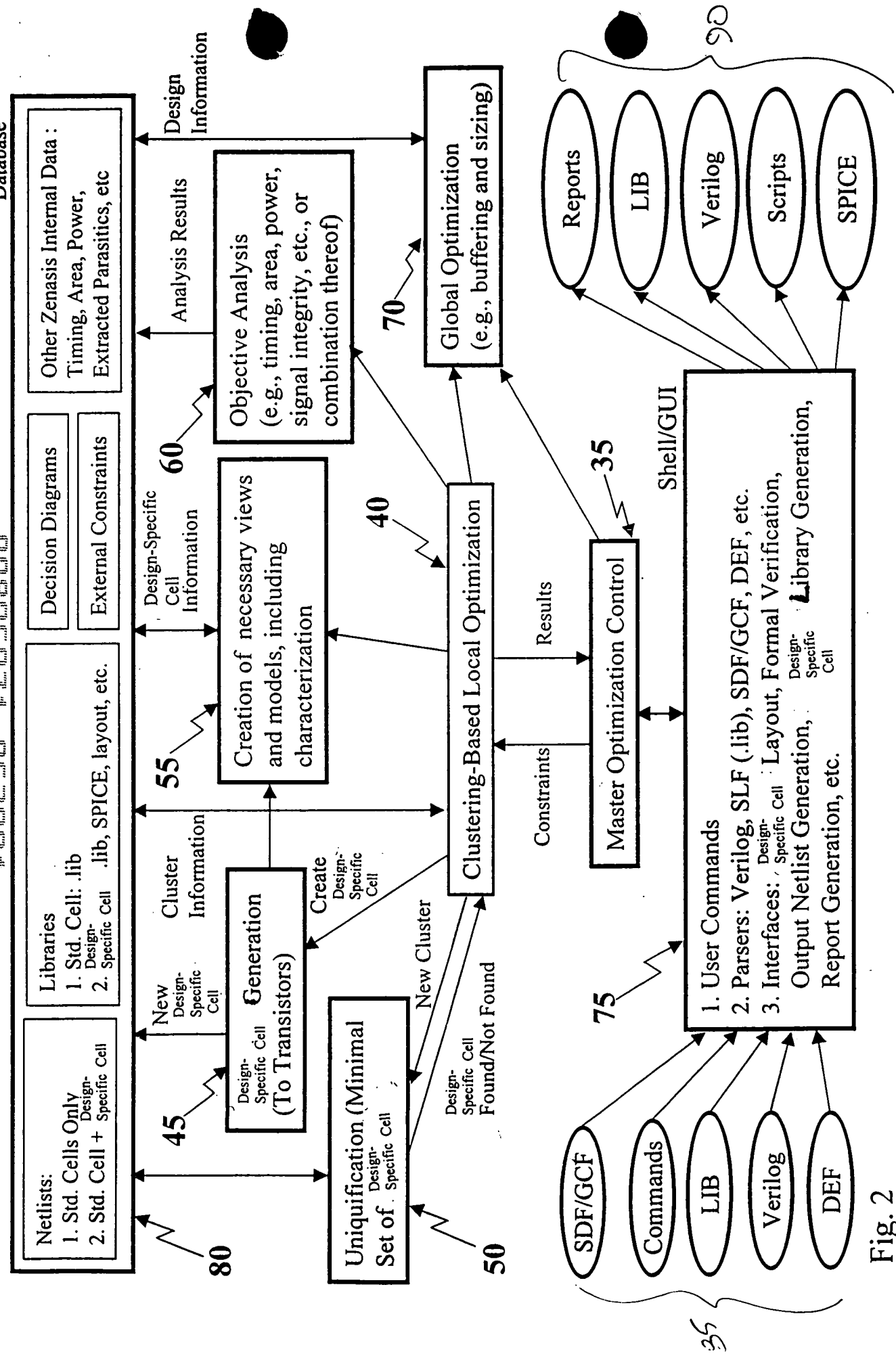


Fig. 2

45

Cluster of standard cells, various context-specific constraints for this cluster, other real-life constraints like process, etc.

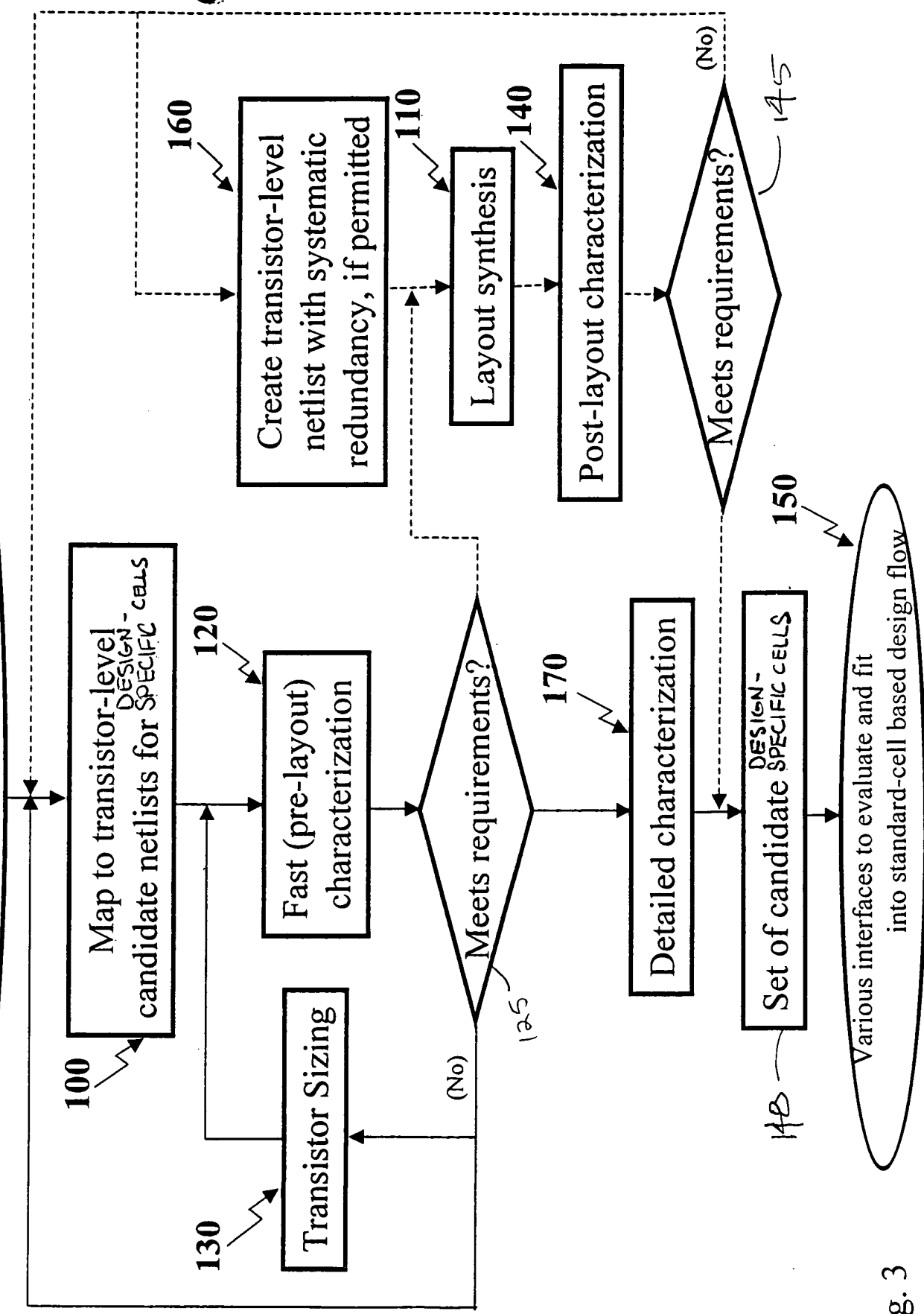


Fig. 3

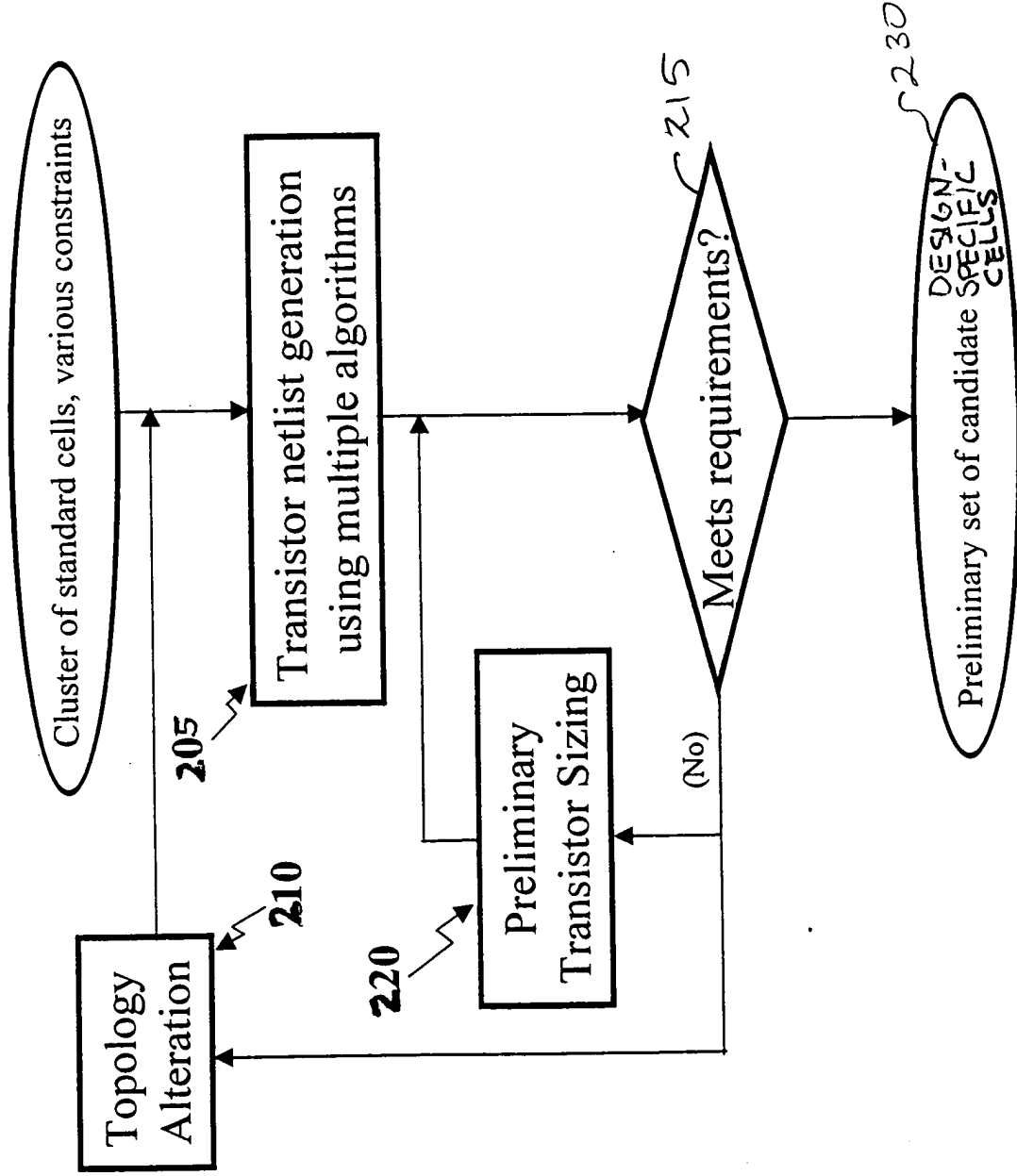
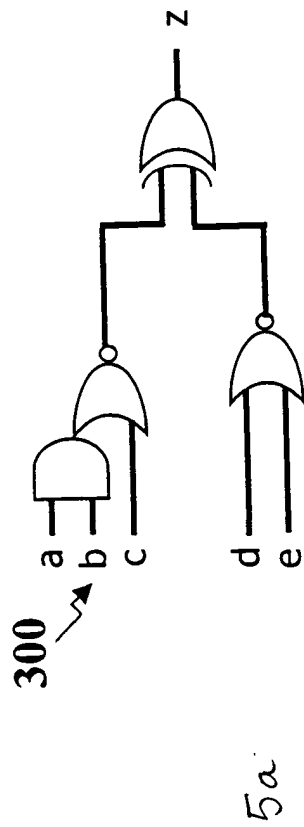


Fig. 4



Critical path to z through b
 ⇒ Delay from b to z : 0.33 ns
 ⇒ Design-SPECIFIC delay : 0.14 ns

5c -

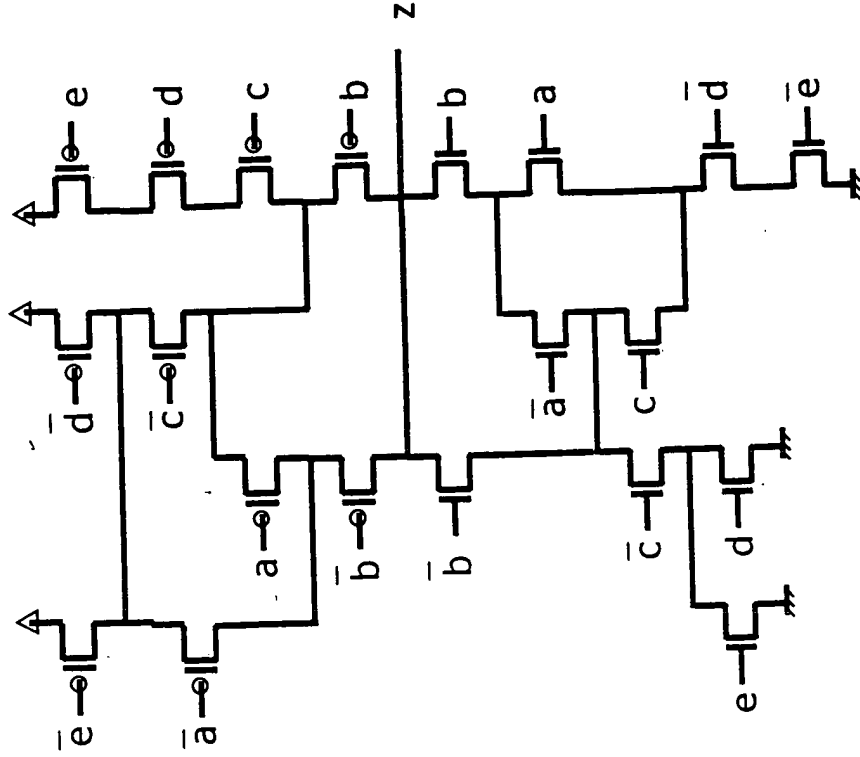
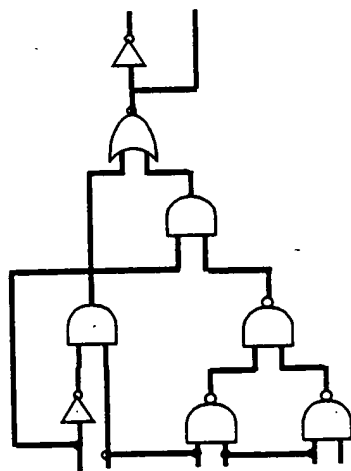
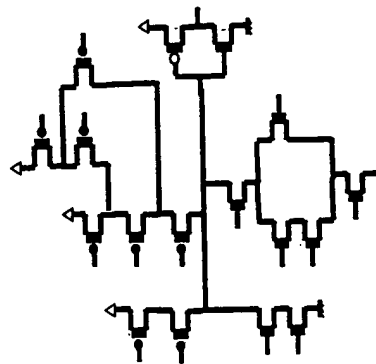


Fig. 5



6a

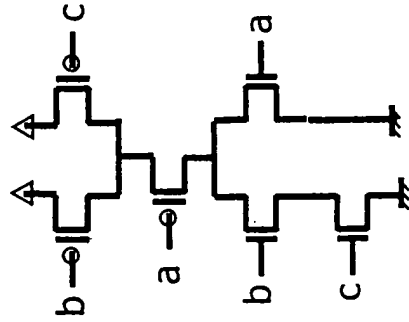
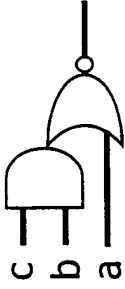


6b

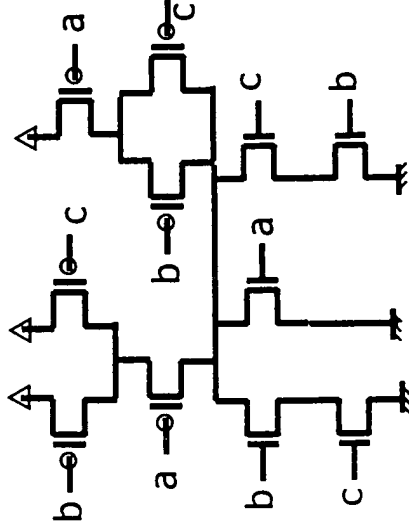
Criteria	Original	Optimized
# of Cells	8	1
# of Transistors	32	17
# of Wires (incl. I/O)	12	5

6c

Fig. 6



Typical standard cell implementation
with no systematic redundancy -- input
a usually has fastest propagation through
cell, c slowest



Implementation of same functionality
with systematic redundancy -- inputs
a and c usually have comparable
propagation delay through module

Fig. 7